DREZNO & LIPSK

THE LEIBNIZ BINARY SUBSYSTEM

BINARY
CONVERSION
KOMPUTOR
& BIT INVERSION
COMMANDER

Models of 1989

OPERATOR'S MANUAL *rev. 1989/1.0*

SALUT

Drezno and Lipsk are the first in series of modules which constitute The Leibniz Binary Subsystem, a group of 8-bit signal processing devices offering comprehensive digital signal manipulation, as well as audio signal, control voltage, trigger, and gate generation. Drezno is the input/output front-end of the system, consisting of an analog–to–digital converter (ADC) and a digital–to–analog converter (DAC), that alone can be used for manipulating analog signals and voltages based on their binary representation (see: 'Binary Code' paragraph). Lipsk (sold separately) is a binary logic processing expander module that can flip (invert) individual bits of the digital signal representation.

INSTALLATION

Drezno requires 12hp worth of free space in the eurorack cabinet. The ribbon type power cable must be plugged into the bus board, paying close attention to polarity orientation. The red stripe indicates the negative 12V rail and should align with the dot, **–12V**, *or* **RED STRIPE** *marks on both the unit and the bus board. The module itself is secured against reversed power connection, however reversing the 16-pin header* **MAY CAUSE SERIOUS DAMAGE** *to other components of your system by short-circuiting the +12V and +5V power rails. There are two connection headers on the back PCB of Drezno for connecting Lipsk or more expansion modules to form an out-in loop (see fig. 3). Lipsk requires 6hp of space, and must be connected to Drezno (and subsequent expanders) using the 10-pin interconnector cable provided. Furthermore, Lipsk requires its own power cable to be connected to the bus board. Both modules should be fastened by mounting the supplied screws before powering up. To better understand these devices, we strongly advise the user to read through the entire manual before using the modules.*

BINARY CODE

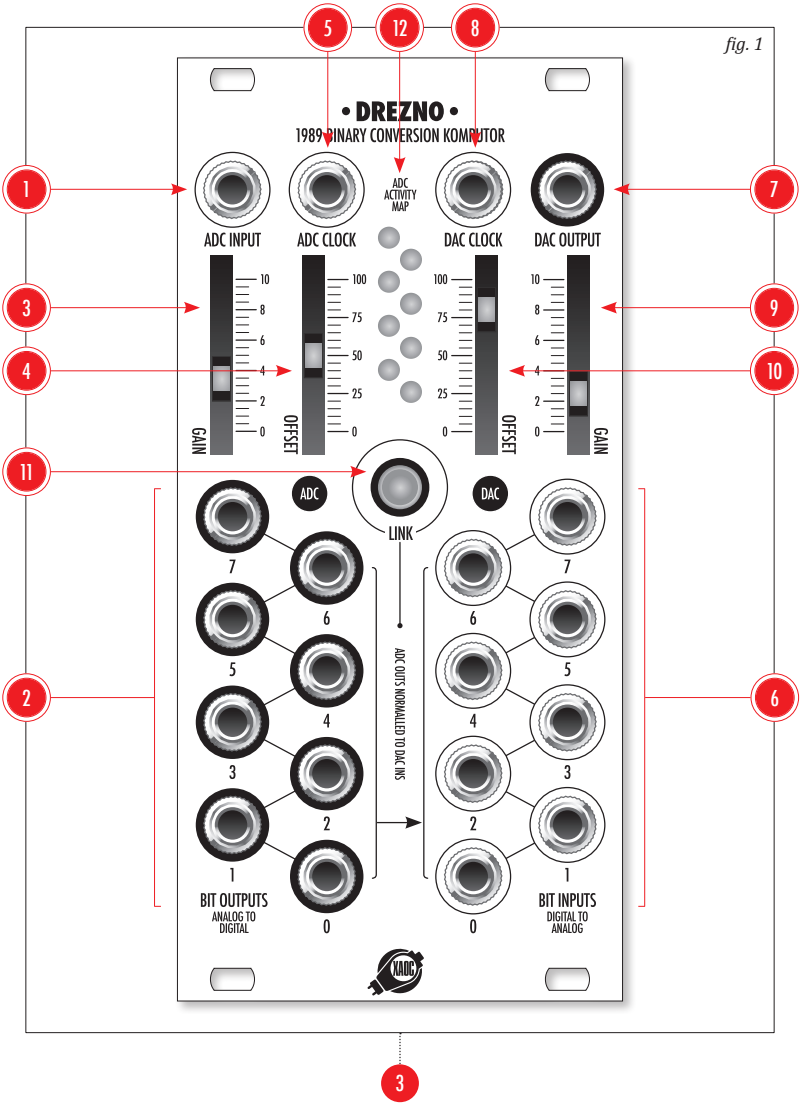
Binary code represents voltage values using patterns of binary symbols (bits), each having one of two possible states: 0 or 1. These bits are organized into strings in order from most significant bit (b_{N-1}) to least significant bit (b_0). For example, a 3-bit code can represent the values 0 (code 000), 1 (code 001), 2 (code 010), 3 (code 011) ... up to 7 (code 111). In an 8-bit system, there are 256 possible values, from 0 (code 00000000) to 255 (code 11111111). The most significant bit (b_7) informs whether the signal value is in the top or bottom half of the range, and each subsequent bit describes the value in greater detail (fig. 4 & 5). In an 8-bit modular synthesis system, the individual bits are represented as gate signals (binary 0=0V, binary 1=5V). Hence the incoming analog voltage is converted into eight gates.

DREZNO CONTROLS AND OPERATION

Drezno consists of two sections (see fig. 1) that can act entirely independently or as a linked pair. The ADC input ❶ *expects either audio or CV signals. There are eight ADC gate outputs* ❷*, representing each of the eight bits,* **7** *to* **0***. The illuminated* **GAIN** ❸ *and* **OFFSET** ❹ *sliders allow the user to adapt the range of the signal fed to the A/D converter. The sliders' respective LEDs indicate signal amplitude and clipping. The A/D converter chip expects only positive voltages, so for bipolar input signals, set the* **OFFSET** *slider to the upper position. The converter is internally clocked at a very high rate (near 2MHz) which helps to avoid aliasing for audio rate signals. The* **ADC CLOCK** *input* ❺ *allows the user to override the internal clock by freezing the output code at the rising edge of the input signal (i.e. gate or trigger). Feeding a pulse wave into the* **ADC CLOCK** *allows the user to control the ADC sampling rate. ADC output activity is indicated by the corresponding set of eight yellow LEDs* ⓬*.*

The DAC section mirrors the ADC section. There are eight DAC gate inputs ❻*, representing each of the eight bits numbered from* **7** *to* **0***. The* **DAC OUTPUT** ❼ *produces a CV or audio signal based on the input code. The* **DAC CLOCK** *input* ❽ *expects gate/trigger signals and is normalized to the ADC clock via the ribbon cable connected to the expander sockets on the back of the module (see fig. 3). Therefore, DAC clock can be replaced by a clock produced by an expander module, and it can be overridden by any signal patched into the panel socket. The DAC section also features* **GAIN** ❾ *and* **OFFSET** ❿ *sliders which*

fig. 1


5
12
8
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2
6
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• DREZNO •
1989 BINARY CONVERSION KOMPUTOR
ADC INPUT
ADC CLOCK
ADC ACTIVITY MAP
DAC CLOCK
DAC OUTPUT
GAIN
OFFSET
OFFSET
GAIN
ADC
LINK
DAC
ADC OUTS NORMALLED TO DAC INS
BIT OUTPUTS
ANALOG TO DIGITAL
BIT INPUTS
DIGITAL TO ANALOG
XAOC

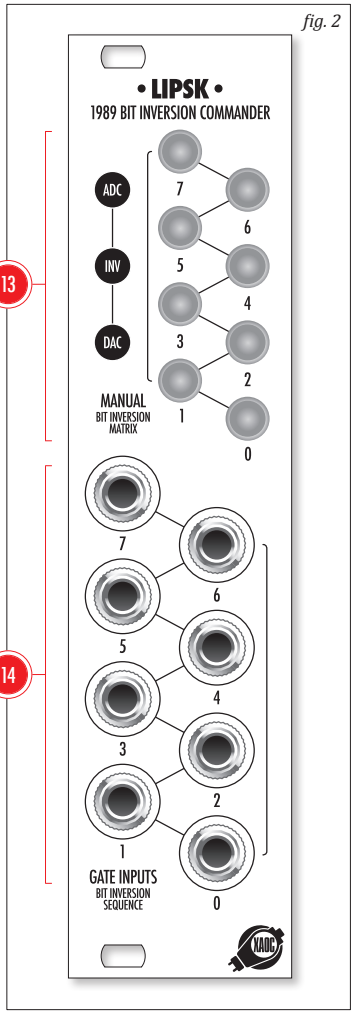


fig. 2

set the level and shift of the DAC output signal. Similarly, their LEDs indicate the amplitude of the output signal and warn against possible clipping at the output stage. To achieve a bipolar output signal, set the **OFFSET** *slider to the lower position.*

The illuminated **LINK** *button* ⓫ *allows the user to connect (normalize) the outputs of the ADC section to the inputs of the DAC section, or—in the case of Lipsk and/or other expanders connected to Drezno—feed the ADC data though the expanders before returning it to DAC. Patching any cable into any DAC binary input breaks its normalization, thereby overriding it with the external signal.*

LIPSK CONTROLS AND OPERATION

Lipsk facilitates the inversion of the individual bits produced by Drezno (or any other module connected to its **IN** *header* ⓯ *on the back), and delivers the resulting code to its* **OUT** *header* ⓰ *(see fig. 3). Bit inversion can be manually controlled by pressing any of combination of its eight illuminated buttons* ⓭*, or it can be automated by patching gate signals into its* **GATE INPUT** *sockets* ⓮*. An active (5V) gate flips the state of the respective bit. If the button is active (bit already flipped), then the gate flips the bit again yielding double inversion (no inversion). The corresponding LEDs show the combined effect of both manual and gate actions. The bit processing logic is hardware-based, so there is virtually no latency, allowing the binary signals to be manipulated at extreme rates..*

SIGNAL MANIPULATIONS AT THE BINARY LEVEL

• When patched 1:1 (or linked without any modifications), processing of signals and voltages through ADC+DAC of Drezno results in a subtle 8-bit quantization effect. Modifying the binary representation creates various discontinuities in the transfer function, depending on which bits are affected. In general, the higher the bit, the more radical the effect of modification. For example, inverting the most significant bit (7) swaps the upper and lower half of the signal, inverting bit (6) swaps odd and even quarters of the range, inverting all bits turns your signal up-

side down. See pages 6-7 for examples of combined inversion of several bits. Even more radical deformations of the signal are achieved by cross-patching individual ADC outputs and DAC inputs. Many interesting, complex waveforms can be obtained when using control voltages from LFOs, envelope generators, and sequencers.

• Bit reduction: a lower-resolution staircase waveform can be created by leaving only higher significant bits (5, 6, 7).

• Bit crushing: this effect can be produced by lowering the input signal level and boosting the output signal level. Bit crushing can be combined with sample rate reduction when using an external clock.

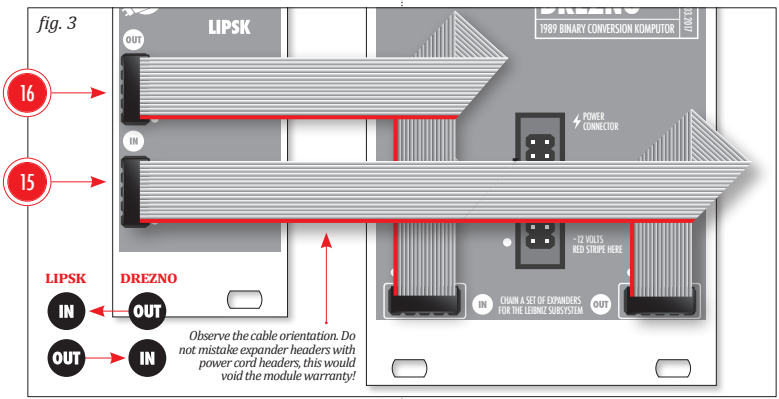
• Generating trigger patterns: feeding an LFO or a sequencer into the ADC provides trigger patterns useful for drum sequencing. The changes on individual outputs can be synchronized by using a higher frequency pulse wave as the ADC clock. This is particularly useful for avoiding the erratic changes that result from the presence of noise in the input signal.

• Frequency multiplier: when a continuous waveform is fed into the ADC, individual binary outputs deliver pulse waveforms that flip between 0V and 5V many times per input period, depending on the level of details they represent. The average frequency of each input is twice as high as the frequency of the input above it, resulting in extremely fast waveforms at the least significant bit (0). **NOTE:** *only input signals with linear slopes (like a sawtooth or triangle) yield uniform rectangular signals at the binary outputs.*

• Interesting waveshapes can be created at the DAC output by feeding the binary DAC inputs with various combinations of gate signals (e.g. taken from binary counters, frequency dividers, or free-running oscillators). The **DAC CLOCK** *input may be employed for freezing the state of the converter at any time, using a single trigger impulse, or a sequence of triggers.*

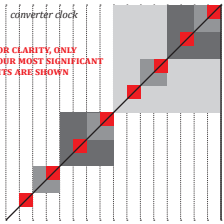
• Drezno (with or without Lipsk connected) can be used in combination with other logic modules (like AND, OR, XOR, etc.), operating on individual bits or entire 8-bit strings. In general, all types of 8-bit mathematical operations may be performed on signals and control voltages in this way. Even more advanced manipulation of signals is possible with two Drezno modules. Combining binary representations of two sources opens a whole universe of transformations that would never be possible with analog signal processing. •

fig. 3

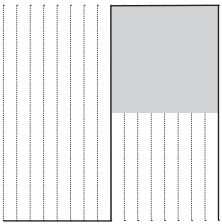


converter clock

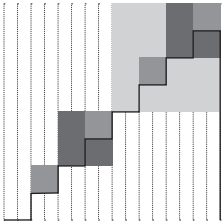
FOR CLARITY, ONLY
FOUR MOST SIGNIFICANT
BITS ARE SHOWN



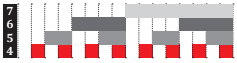
input saw wave and significance of individual bits

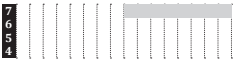


result of leaving only the most significant bit (7)

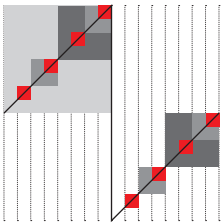


result of leaving three most significant bits (7, 6, 5)

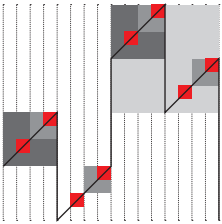




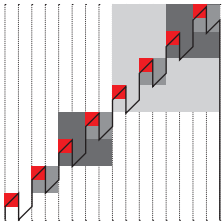
gate signals at individual bit outputs



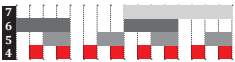
result of inverting the most significant bit (7) only



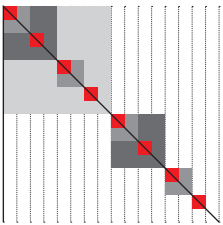
result of inverting bit (6) only



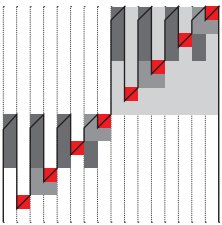
result of inverting bit (4) only



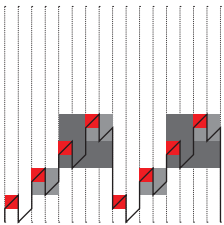
gate signals at individual bit outputs



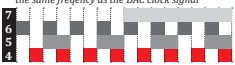
waveform obtained by inverting all bits



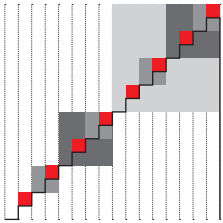
replacement of bit (6) with square waveform of the same freqency as the DAC clock signal



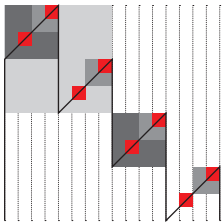
inversion of bit (4) and omission of bit (7)



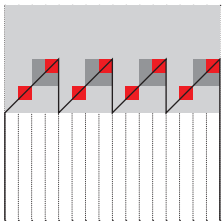
gate signals at individual bit outputs



result of four most significant bits (7, 6, 5, 4)



result of inverting two most significant bits (7, 6)



replacement of bit (7) by external gate and omission of bit (6)

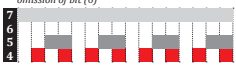


fig. 4:
INPUT SINUSOIDAL SIGNAL AND INDIVIDUAL BINARY GATES

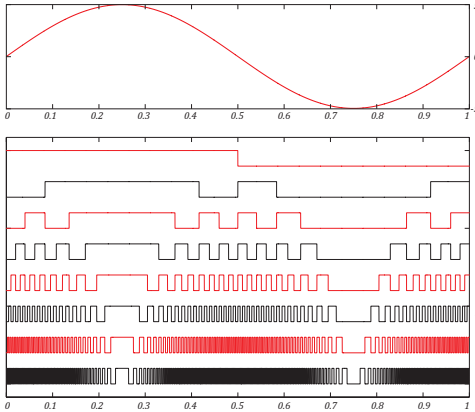
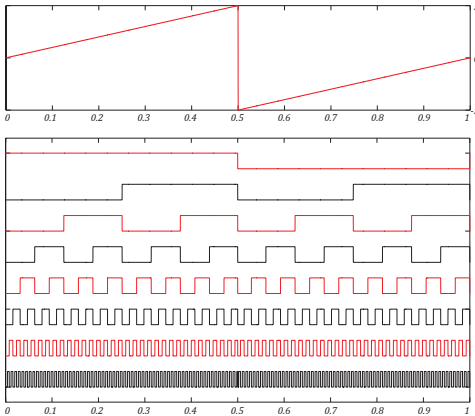


fig. 5:
INPUT SAWTOOTH SIGNAL AND INDIVIDUAL BINARY GATES



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EASTERN BLOC TECHNOLOGIES

RADA WZAJEMNEJ POMOCY GOSPODARCZEJ

MADE IN THE EUROPEAN UNION

MAIN FEATURES

Universal subsystem for creating and processing analog signals in the 8-bit digital domain

Suitable for CV and audio processing with no aliasing

Independent ADC & DAC

Near 2Mhz internal clock with external clock inputs to both converters

Lipsk: bit inversion with manual and CV gate control

TECHNICAL DETAILS

Drezno is 12hp, Lipsk is 6hp, both skiff friendly

Drezno current draw: +50mA/-35mA

Lipsk current draw: +30mA/-0mA

Reverse power protection